Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of operating a processor comprising:

in a single clock cycle, concatenating a first word and a second word to produce an intermediate result;

shifting the intermediate result by a specified shift amount; and

storing the shifted intermediate result in a third word.

2. ~~(Original) The method of claim 1 wherein the first word and the second word and the third word are 32-bit words.~~

3. ~~(Original) The method of claim 1 wherein the intermediate result is a 64-bit word.~~

4. (Original) The method of claim 1 wherein shifting comprises right shifting.

5. (Original) The method of claim 4 wherein the specified shift amount is in an operand.

6. (Original) The method of claim 4 wherein the specified shift amount is a value between one and thirty-one.

7. (Original) The method of claim 4 wherein the specified shift amount is a value contained in a lower five bits of the first word.

8. (Currently Amended) A computer instruction comprising:

in a single clock cycle, an instruction to concatenate a first word and a second word to produce an intermediate result;

shift the intermediate result by a specified amount; and

store the shifted intermediate result in a third word.

9. (Original) The instruction of claim 8 wherein the first word and the second word and the third word are 32-bit words.

10. ~~(Original) The instruction of claim 8 wherein the intermediate result is a 64-bit word.~~

11. (Original) The instruction of claim 8 wherein shifting comprises right shifting.

12. (Original) The instruction of claim 11 wherein the specified amount is in an operand.

13. (Original) The instruction of claim 11 wherein the specified amount is a value between one and thirty-one.

14. (Original) The instruction of claim 11 wherein the specified amount is a value contained in a lower five bits of the first word.

15. (New) A method comprising:

in a single cycle in a parallel hardware-based multithreaded processor, concatenating a first 32-bit operand and a second 32-bit operand to produce a 64-bit concatenation result;

right shifting the 64-bit concatenation result by a specified amount; and

storing a lower 32 bits in a destination register.

16. (New) The method of claim 15 in which the first 32-bit operand is a context-relative register name.

17. (New) The method of claim 15 in which the second 32-bit operand is a context-relative register name.

18. (New) The method of claim 15 in which the specified amount is a value from 1 to 31.

19. (New) The method of claim 15 in which the destination register is an absolute register name.

20. (New) The method of claim 15 in which the destination register is a context-relative register name.